SpotSDC: An Information Visualization System to Analyze Silent Data Corruption

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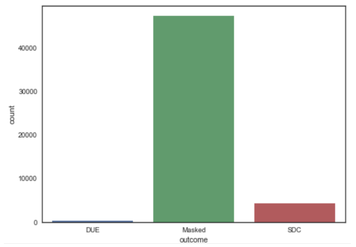
Abstract: The aggressive scaling trend in high-performance computing architectures increases the probability of silent data corruption (SDC) and reduces result reliability. Understanding how SDC affects an application is critical for developing suitable techniques and improving application's resilience. In this work, we design SpotSDC, a visualization system to aid users in understanding the impact of silent data corruption on HPC programs.

Motivation

Technology scaling trends have made hardware more susceptible to transient faults which may cause:

- ***DUE***: The hardware error causes the program to crash
- ***Masked***: The final error in the program output is too small to matter
- ***SDC***: The hardware error silently corrupts the data, which leads to undetected yet significant computation error

Current approaches for studying fault injection provide only a partial information about impact of transient faults.



Outcome distribution in conjugate gradient test program

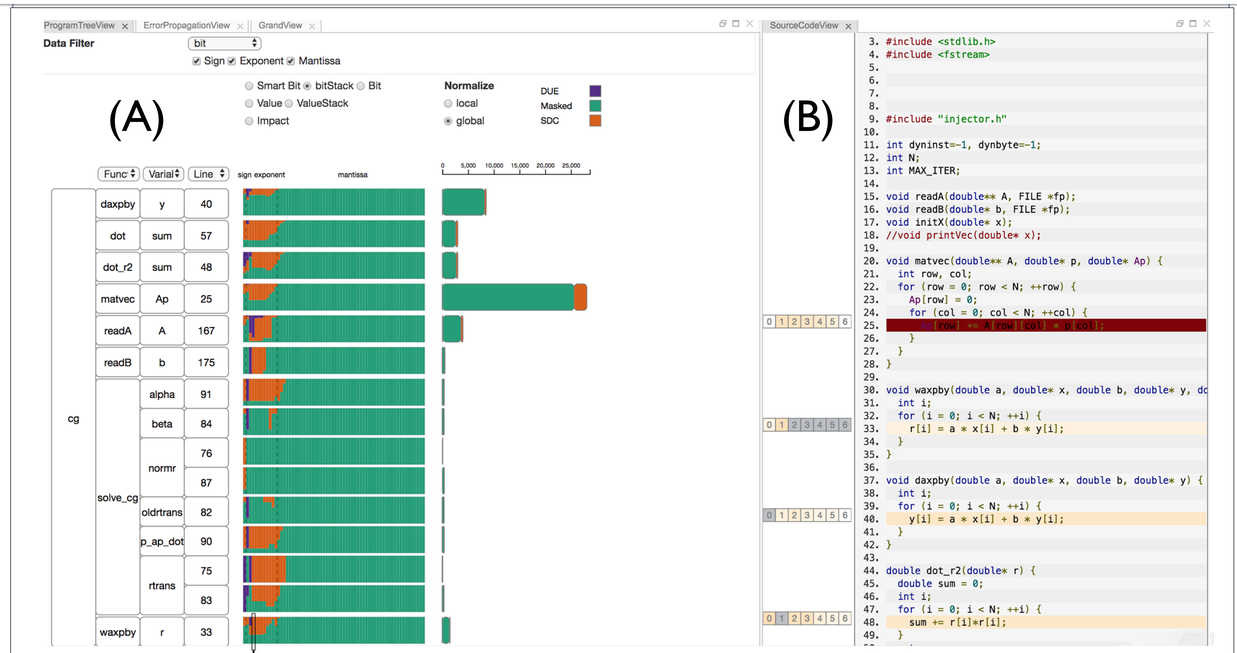
A domain specific visualization system is needed to provide a detailed picture of impact of silent data corruptions and how they propagate through an application.

Objective

Design a visualization system to understand the impact of transient faults and study their propagation through an application.

Data Description

The data set applies to SpotSDC is collected from a fault injection campaign. For each fault injection experiment, we record when, where a fault is injected, the injected location's ground truth value, the corrupted value, and the number of flipped bit. In each fault injection experiment, we also record all critical variables' value during program execution.



Here, we study the fault vulnerability of a conjugate gradient benchmark(CG). We performed an exhaustive fault injection study with a single bit-flip fault model and analyze the results with SpotSDC.

(A) SpotSDC Overview Visualization

We see that CG line 25 consumes a large amount of execution time and has a high SDC rate. The majority of the errors resulting in SDC is due to bit flips in exponent bits.

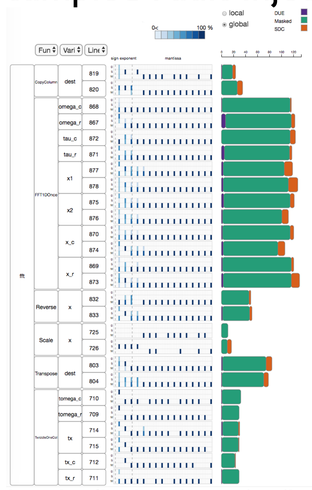
(B) Source Code Visualization

Line 25 of CG is the most vulnerable to SDC, but as the iterations progress the SDC impact decreases.

(C) Propagation Visualization

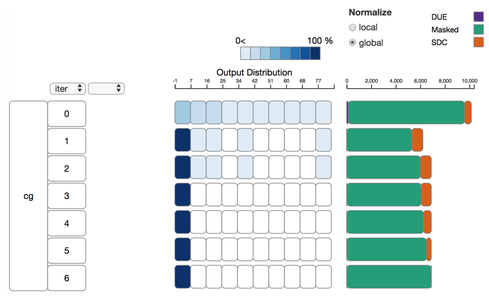
An error is injected during the execution at line 33 into variable r. The error propagates to the array variable Ap in line 25.

Visualization Overview for Sub-sampled Fault Injection



- The overview visualization shows the distribution of sub-sample with respect to the functions, variables and lines.
- It identifies the regions where more fault injection samples are required for better fidelity.

The Impact of a Bit Flip Relative to the Iteration Number



- Errors in the initialization phase leads to wide range of errors in the output.
- Errors in early iterations may lead to more SDC than later iterations.

Reference

Menon, Harshitha, and Kathryn Mohror. "DisCVar: discovering critical variables using algorithmic differentiation for transient faults." *Proceedings of the 23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*. ACM, 2018.

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